source and drain regions located in the silicon carbide tub and laterally offset from the gate; and

a complimentary metal-oxide semiconductor (CMOS) device formed on the conductive substrate, the CMOS device having a tub comprising a material different from the silicon carbide tub, and wherein the conductive substrate includes a buried oxide layer formed therein.--

## REMARKS

The Applicants have carefully considered this Application in connection with the Examiner's Action, and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-43 in the Application. In response to a restriction requirement, the Applicants previously elected Claims 1-10 and withdrew Claims 11-43 from consideration pending the filing of a Divisional Application. The Applicants subsequently canceled Claims 1-10, without prejudice or disclaimer, and added new Claims 44-54. Thereafter, the Applicants canceled Claim 48 without prejudice or disclaimer. Accordingly, Claims 44-47 and 49-54 are currently pending in the Application.

### I. Rejection of Claim 48 under 35 U.S.C. §112

The Examiner maintains his rejection under 35 U.S.C. §112, first paragraph, that Claim 48 contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors had possession of the claimed invention at the time the application was filed. Specifically, the Examiner maintains that there is no support for a SiC tub

located within a trench, as previously recited in Claim 48, since the embodiment of Fig. 3 does not disclose forming a trench. The Examiner's argument is without support for a number of reasons.

First, Claim 48 was previously canceled without prejudice or disclaimer in the response to the October 11, 2002, Examiner's Action. Thus, it is no longer pending in the case. Second, even though Claim 48 was previously rolled into independent Claim 44, the Application does provide support for the trench. In support of this, the Applicants currently present Fig. 2F and its supporting text from the application as filed.

*FIG. 2F*

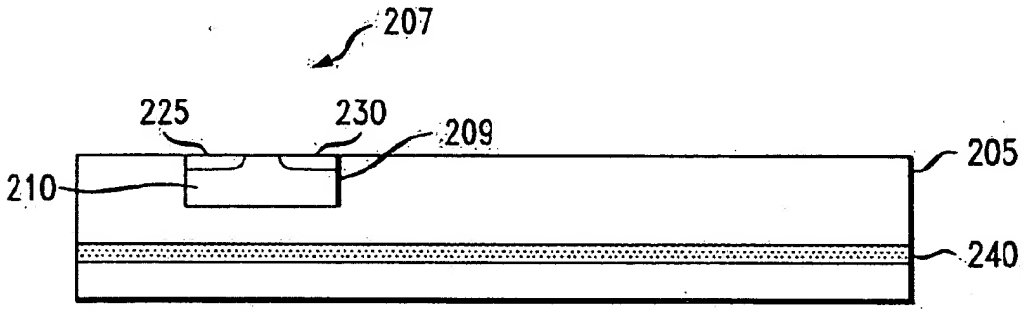



FIGURE 2F illustrates still another embodiment, in which the MOSFET device 200 may be formed within a substrate 205 having an insulator layer 240 formed therein, which was discussed in FIGURE 2E. In such embodiments, a silicon trench 209 is conventionally formed in the substrate 205 prior to the formation of the silicon carbide layer 210. The silicon carbide layer 210 is then deposited in the silicon trench 209. Of course, another embodiment of the present invention may form the silicon trench 209 and the silicon carbide layer 210 within a substrate that does not have the insulator layer 240. Following the formation of the silicon carbide layer 210, a gate is formed on the silicon carbide layer 210 in the manner discussed herein for other embodiments. (Page 16, line 16 thru page17, line 4 of the application as filed).

Thus, the embodiment of Fig. 2F illustrates a silicon trench 209 in which a SiC tub 210 is formed. The specification goes on further to say that the substrate is a silicon substrate. Accordingly, Fig. 2F taken together with the remainder of the present application reasonably conveys to one skilled in the art that a silicon carbide tub may be located within a trench formed in a conductive substrate, as previously recited in Claim 48 and now incorporated in independent Clam 44. Therefore, the Applicants respectfully traverse the Examiner's rejection of the subject matter of previous Claim 48 under 35 U.S.C. §112, first paragraph.

## II. Rejection of Claims 44-47, 49-51 and 53 under 35 U.S.C. §103

The Examiner has rejected Claims 44-47, 49-51 and 53 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,896,194 to Suzuki in view of U.S. Patent No. 5,672,889 to Brown. However, the combination of Suzuki and Brown fails to support a *prima facie* case of obviousness of Claim 44 and its dependent claims because the combination fails to teach or suggest each and every element recited in Claim 44.

More specifically, the combination fails to teach a silicon carbide tub located within a trench formed in a conductive substrate, as recited in Claim 44, and as conceded by the Examiner. (Examiner's Action, page 5). However, the Examiner asserts that it would have been obvious to a person of ordinary skill in the art to form the GaAs layer 31 in the Si substrate 32 rather than on the substrate 32, as disclosed in Suzuki. The Applicants respectfully disagree. The GaAs layer 31 cannot practically be formed in a trench in the substrate 32 because a substantial portion of the substrate 32 underlying the GaAs layer 31 is removed to form a hole 33 after the GaAs layer 31 is

deposited on the substrate 32. (Column 3, lines 48-68). Forming the GaAs layer 31 in a trench in the substrate 32 and subsequently removing most of the portions of the substrate 32 under the trench would result in a device that was mechanically unsound and excessively susceptible to failure due to the lack of support of the GaAs layer 31 within the substrate 32. Thus, it is not obvious to a person of ordinary skill in the art to form the GaAs layer 31 in a trench in the substrate 32.

Brown also fails to teach or suggest forming a silicon carbide tub within a trench formed in a conductive substrate, as recited in Claim 44 of the present application. In contrast, Brown merely teaches forming a number of different SiC layers 10, 12, 14 over one another, and then forming grooves 16 through at least two of the three SiC layers 10, 12, 14. (Column 5, lines 9-15). Thus, where the present invention requires the element of a silicon carbide tub located within a trench formed in a conductive substrate, Brown only discloses three SiC layers, one of which forms a silicon carbide tub. While Brown might teach trenches or grooves, the only material located within those trenches and groves in Brown are oxides and gate electrodes, but not the silicon carbide required by the present invention. Therefore, Brown also fails to teach or suggest that a silicon carbide tub is located within a trench in a conductive substrate, as presently claimed.

Moreover, because Brown is directed toward vertical transistors instead of horizontal transistors, one skilled in the art would find no suggestion, motivation or even mere mention of forming the SiC channel layer 12 in a trench in a substrate because a channel layer formed in a trench would cover or otherwise restrict access to the underlying source or drain and render the transistor inoperable.

Accordingly, the combination of Suzuki and Brown fails to teach or suggest each and every

element of Claim 44 of the present application. In view of the foregoing remarks, the combination of Suzuki and Brown fails to support a *prima face* case of obviousness of Claims 44-47, 49-51 and 53 under 35 U.S.C. §103(a). Consequently, the Applicants request the Examiner withdraw the §103 rejection of Claims 44-53.

## III. Rejection of Claims 52 and 54 under 35 U.S.C. §103

The Examiner has rejected Claims 52 and 54 under 35 U.S.C. §103(a) as being unpatentable over Suzuki and Brown as applied to Claim 44 above, and further in view of U.S. Patent No. 5,326,991 to Takasu. However, the combination of Suzuki, Brown and Takasu fails to support a *prima facie* case of obviousness of Claims 52 and 54 because the combination fails to teach or suggest each and every element recited therein. More specifically, the combination fails to teach a conductive substrate that includes a buried oxide layer formed therein, as recited in Claims 52 and 54.

The Examiner asserts that it would have been obvious to a person of ordinary skill in the art to form a combination of the Suzuki and Brown devices on a SOI substrate as taught by Takasu in order to improve the electrical isolation of the device. The Applicants respectfully disagree.

As the Examiner concedes, neither Suzuki nor Brown teaches the insulator layer. Further, one skilled in the art would not be motivated to employ a SOI substrate as taught by Takasu with the teachings of Suzuki, as asserted by the Examiner. More specifically, after forming the GaAs layer 31 on the Si substrate 32, Suzuki teaches forming a hole 33 that terminates at the GaAs layer 31, wherein the sides of the hole 33 and the exposed, bottom surface of the GaAs layer 31 are

subsequently lined with a metal layer 34 comprising a Ti/Au stack. (Column 5, lines 50-55). The metal layer 34 electrically connects the top and bottom sides of the device. One skilled in the art would not employ a SOI substrate or another substrate having a buried oxide layer therein when both sides of the substrate are electrically coupled to one another, because this would destroy the intended conductivity of the device. Thus, Suzuki fails to suggest employing a substrate having a buried oxide layer formed therein, as recited in Claims 52 and 54 of the present application. Accordingly, the Applicants respectfully traverse the Examiner's assertion that it would have been obvious to one skilled in the art to construct the Suzuki device on a SOI substrate as taught by Takasu.

Therefore, the combination of Suzuki, Brown and Takasu fails to teach or suggest each and every element of Claims 52 and 54 of the present application. In view of the foregoing remarks, the combination fails to support a *prima face* case of obviousness of Claims 52 and 54 under 35 U.S.C. §103(a).

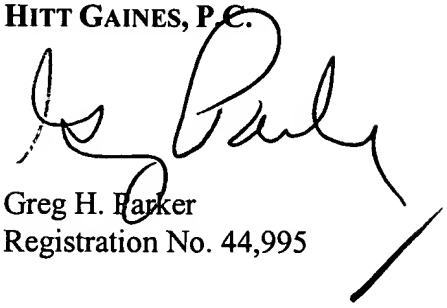
## IV. Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 44-53. The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present

application.

Respectfully submitted,

**HITT GAINES, P.C.**



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